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Certified by

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Provisional Patent Application for

OPTIMIZED CONTACT DESIGN FOR THERMOSONIC BONDING OF FLIP-CHIP DEVICES

I. SUMMARY

The manufacture of high lumen output InGaN LEDs benefits from flip chip packaging. In a flip chip InGaN LED, desirable characteristics for die attachment include low thermal resistivity and structural robustness. Both of these can be fulfilled by using thermosonic (TS) bonding for packaging. However, the TS bonding process can present its own challenges, e.g., maintaining good contact across the chip area. Accordingly, an aspect of the present inventive subject matter proposes a contact methodology for optimizing light extraction and manufacturability for thermosonically bonded InGaN LEDs.

II. PROBLEM

Traditionally, InGaN LEDs have been packaged with the substrate down on a heat sink; here, light is extracted from the LED through current spreading, semi-transparent layers deposited on the p-type layer. The overall extraction efficiency of the device is lowered due to light absorption in the current spreading layer.

An alternative method to packaging would be to use the flip chip geometry in which light extraction is primarily through the substrate. It has been shown that a 60% increase in extraction efficiency can be obtained by flipping the InGaN LED on a sapphire substrate. Solder bumps (> approx. 50 μm) are typically used to attach the chip to the submount (Figure 1). For packaging InGaN LEDs, solder attachment has its own merits and drawbacks. One advantage is that the large thickness of the solder tends to planarize; thus, limited restrictions are placed on the difference in thickness between the p & n-contacts. Solder attachment of chip to submount, however, suffers from high thermal resistance; in addition, since it is often the first step of the packaging process, a high reflow temperature needs to be used (> approx. 250° C) and this may compromise the reflectivity of the p-contact. In addition, solder processes typically require cleaning of flux residue after bonding. Cleaning solution or residual flux may compromise reliability by creating a leakage path through resistive shunt.

Alternative packaging technologies are therefore of interest. TS bonding with Au bumps is one such technology; it enables the chip to be attached to the submount with ultrasonic energy,

without any intermediate melting/re-solidification step. Consequently, lower packaging temperatures (around 150° C) can be used, thus avoiding any loss of reflectivity of the p-contact. In addition, the use of Au bumps instead of solder, lowers the thermal resistance of the package. In TS bonding, deformation of Au bumps and physical bonding of Au bumps on submount to the Au –terminated p & n-bump areas on the chip occurs. Consequently, the p & n-bump areas on the chip should be more or less at the same elevation (Figure 2) (i.e., within the extent of deformation of the bumps); consequently, in a typical chip, a significant amount of the light exiting the mesa, gets absorbed by the n-trace on the chip (same elevation as the n-bump area on the chip). This causes significant light loss.

In many prior art designs, n-trace consists of several electrically separate pieces, interconnected only on submount level. If the chip or submount planarity is imperfect, one of such pieces may not be firmly connected to the bumps, resulting in higher electrical resistance of that piece and current spreading non-uniformity.

In accordance with the present inventive subject matter, contact methodologies that minimize light loss in LED chips packaged using thermosonic/thermocompression bonding are proposed.

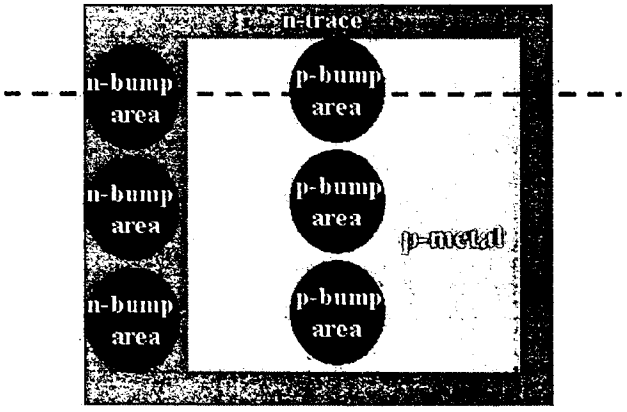

Fig. 1a. Top layout of a typical flip chip.

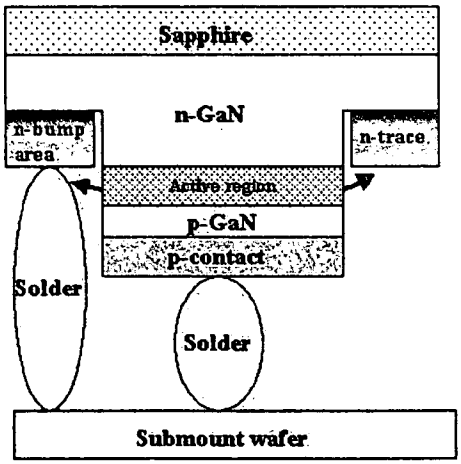

Fig. 1b. Chip attached to submount with solder. While light (indicated by arrows) exiting towards the bumps, does get trapped, light exiting the active region away from the bumps, leaves with minimal loss.

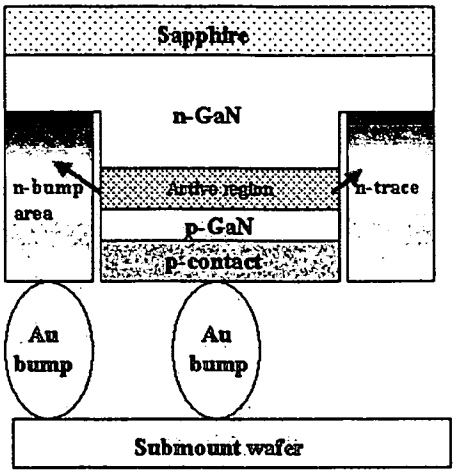

Fig. 2. Chip attached to submount by TS bonding. Unlike the chips attached with solder, light (indicated by arrows) exiting the active region away from the bumps, also gets trapped since the n & p-metal are at the same height to enable uniform bonding.

III. OBJECT

The present inventive subject matter is directed to a contact methodology for minimizing light loss and improving manufacturability for thermosonically bonded InGaN LEDs.

IV. DESCRIPTION OF PREFERRED EMBODIMENT(S)

At first glance, it might appear from Figures 1 & 2 that the easiest way to minimize light loss is to eliminate the n-trace, i.e., not have any n-metal outside of the n-attachment area (Figure 3). However, this can lead to poor current spreading and non-uniform light emission; most of the light would then be emitted from the p-area closest to the n-metal.

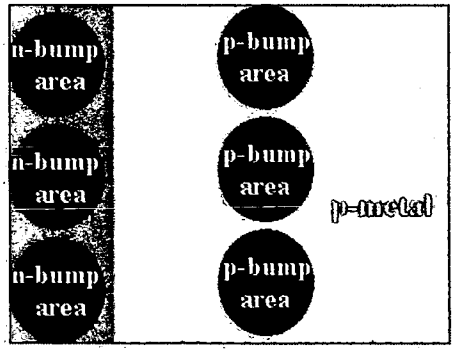

Figure 3.

In accordance with aspect of the present inventive subject matter, 3 general features and several die layouts are proposed which optimize current spreading with minimum light loss and ease of

die attach for thermosonically bonded LEDs. One feature is eliminating n-trace metal on the outside of the chip, but still maintaining adequate current spreading with an n-metal network in the interior of the chip. The current spreading is further enhanced, by having n-GaN with low resistivity (typically < 20 ohms/square). This design also results in n-bump areas being completely surrounded by p-bump areas & thus, reduces the problems associated with variation of p & n-bump heights on the submount; in effect, it is more mechanically robust, unlike the design shown in Figure 1a. Additional improvement of die attach manufacturability is achieved by connecting all n-traces together in a continuous network to avoid imperfect connections to pieces of n-trace. Robustness is further improved by the third feature – p- and n-bump having approximately level top surfaces. If the difference of surface levels of the bumps is within the deformation range of the top Au layer on the bump, reliable connection across the chip is achieved reproducibly.

In Figure 4, we show three die layouts based on the above design rules.

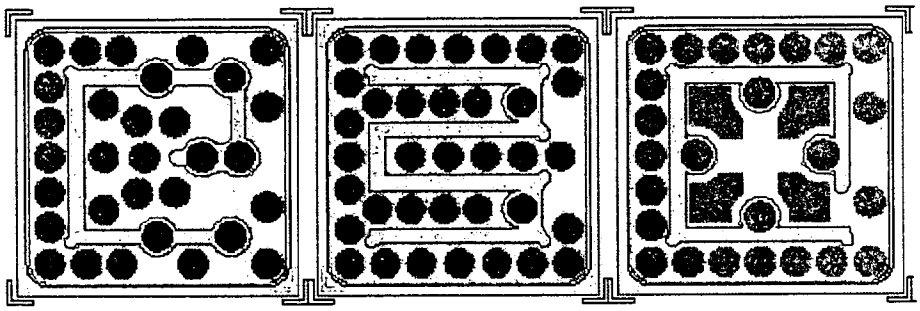

Figure 4. Mechanically robust die designs which minimize light loss in thermosonically bonded InGaN LEDs. Note, the bump areas are shown in red, the n-traces are shown in yellow, and the p-metal is shown in blue.

In a preferred embodiment of the invention, after mesa formation, the p-contact metal would be deposited on the p-GaN contact layer. The n-contact is then defined and the device is protected with dielectric, along with definition of p-bump & n-bump areas. The device is annealed at 250° C. After separation, the individual dies are ready for flip bonding and subsequently thermosonically bonded to a submount, with Au-terminated bumps.

V. TEST DATA

The dies with designs shown in Figure 4 have been attached to Au-terminated submount and shown to have excellent mechanical robustness, when compared to the design shown in Figure 1a. In addition, the entire p-mesa lights up under forward bias, indicating uniform light emission, good current spreading and good contact at both the p & n-regions of the chip with the submount. This design has also been demonstrated to result in a low thermal resistance at the chip/submount interface.

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PROVISIONAL APPLICATION FOR PATENT COVER SHEET

This is a request for filing a PROVISIONAL APPLICATION FOR PATENT under 37 CFR 1.53(c).

MAIL STOP PROVISIONAL APPLICATION
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Transmitted herewith for filing is the Provisional Patent Application of:

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Title of the invention:

OPTIMIZED CONTACT DESIGN FOR THERMOSONIC BONDING OF FLIP-CHIP DEVICES

Enclosed application parts (*check all that apply*)

- ☒ 4 Pages of Specification Including Five (5) Figures
- ☐ _____ Page of Abstract
- ☐ Application Data Sheet
- ☐ CD(s)
- ☐ Other (specify) _____

Method of Payment of Filing Fees for this Provisional Application for Patent:

- ☐ Applicant claims *small entity* status. See 37 CFR § 1.27.
- ☒ A check is enclosed to cover the filing fees.
- ☒ The Commissioner is hereby authorized to charge filing fees or credit any overpayment to Deposit Account No. 06-0308.

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☒ No
☐ Yes, the name of the U.S. Government agency and the Government contract number are:

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Date of Deposit: December 24, 2003

I hereby certify that this *PROVISIONAL APPLICATION FOR PATENT COVER SHEET* and accompanying papers are being deposited with the United States Postal Service "Express Mail Post Office To Addressee" service under 37 C.F.R. 1.10 on the date indicated above and is addressed to the MAIL STOP PROVISIONAL APPLICATION, Commissioner For Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

Mary Ann Temesvari